Georgia Institute of Technology

School of Electrical and Computer Engineering

ECE 3043 Electrical and Electronic Circuits Laboratory Verification Sheet

NAME:_____ SECTION:_____

AD LOGIN:_____

Experiment 12: BJT CE Amplifier

Procedure	Time Completed	Date Completed	Verification (Must demonstrate circuit)	Points Possible	Points Received
3. Bias				25	
4,5. Small Signal Gain and Freq Response				25	
6. Clipping				25	
7. Spectral Analysis				25	

To be permitted to complete the experiment during the open lab hours, you must complete at least **four** procedures during your scheduled lab period or spend your entire scheduled lab session attempting to do so. A signature below by your lab instructor, Dr. Brewer, or Dr. Robinson permits you to attend the open lab hours to complete the experiment and receive full credit on the report. Without this signature, you may use the open lab to perform the experiment at a 50% penalty.

SIGNATURE:_____ DATE:_____

ECE 3043 Check-off Requirements for Experiment 12

Make sure you have made all required measurements before requesting a check-off. For all check-offs, you must demonstrate the circuit or measurement to a lab instructor. All screen captures must have a time/date stamp.

4. Bias
   - ✓ Collector, base, and emitter voltages and collector current recorded.

5, 6 . Gain and Frequency Response
   - ✓ Oscilloscope screen capture showing input and output signals and Vpp measurements for each signal.
   - ✓ Calculation of the gain.
   - ✓ Plot of gain versus frequency made with HPVEE, LabView, or by hand with -3dB frequencies and midband gain labeled and their values recorded.

7. Clipping
   - ✓ Screen capture showing soft clipping on output and measured positive and negative peak amplitudes (can use max and min functions on scope).
   - ✓ Screen capture showing hard clipping on output and measured positive and negative clipping levels (can use max and min functions on scope).
   - ✓ Screen capture of XY plot when amplifier is clipped.
   - ✓ Calculation of slope of XY plot (use scope cursors).

8. Spectral Analysis
   - ✓ Screen capture showing fundamental and distortion components of output signal. Increase input if necessary to generate distortion components. The output should not be clipped.
   - ✓ Screen capture after adjusting pot to maximize amplitude of fundamental but eliminate distortion components.
   - ✓ Screen capture of input and output sine waves after pot adjustment.
   - ✓ Measured circuit gain after pot adjustment.
   - ✓ Measured pot value (disconnect pot from circuit before measuring).

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COMMON EMITTER AMPLIFIER LTSPICE EXAMPLE
VI 1 0 AC 1 SIN(0 0.7 1K)
*VOLTAGE SOURCE FOR EITHER AC OR TRAN ANALYSIS, ARGUMENTS OF SINE DC LEVEL, AMPLITUDE, FREQ
RB1 2 0 27K
RB2 6 2 150K
RE1 4 0 2K
RE2 4 7 100
RC 6 3 10K
RL 5 0 20K
C1 1 2 0.22U
C2 3 5 10U
CE 7 0 100U
Q 3 2 4 QKITTYCAT
VPLUS 6 0 DC 15
.MODEL QKITTYCAT NPN(IS=10F BF=200 VA=170 CJC=3.6P TF=0.3N RB=10)
*IS SATURATION CURRENT, BF FORWARD BETA, VA EARLY VOLTAGE,
*CJC COLLECTION JUNCTION CAPACITANCE, TF FORWARD TRANSIT TIME,
*RB BASE SPREADING RESISTANCE
*DO ONE ANALYSIS AT A TIME. PUT AN ASTERISK IN FRONT OF THE OTHERS
*.OP
*OP PROVIDES THE Q POINT
.AC DEC 300 10 100MEG
*.TRAN 0 3M
*.FOUR 1K V(5)
*FOURIER ANALYSIS OF VOLTAGE AT NODE 5 WITH 1K AS FUNDAMENTAL FREQUENCY
.PROBE
.END
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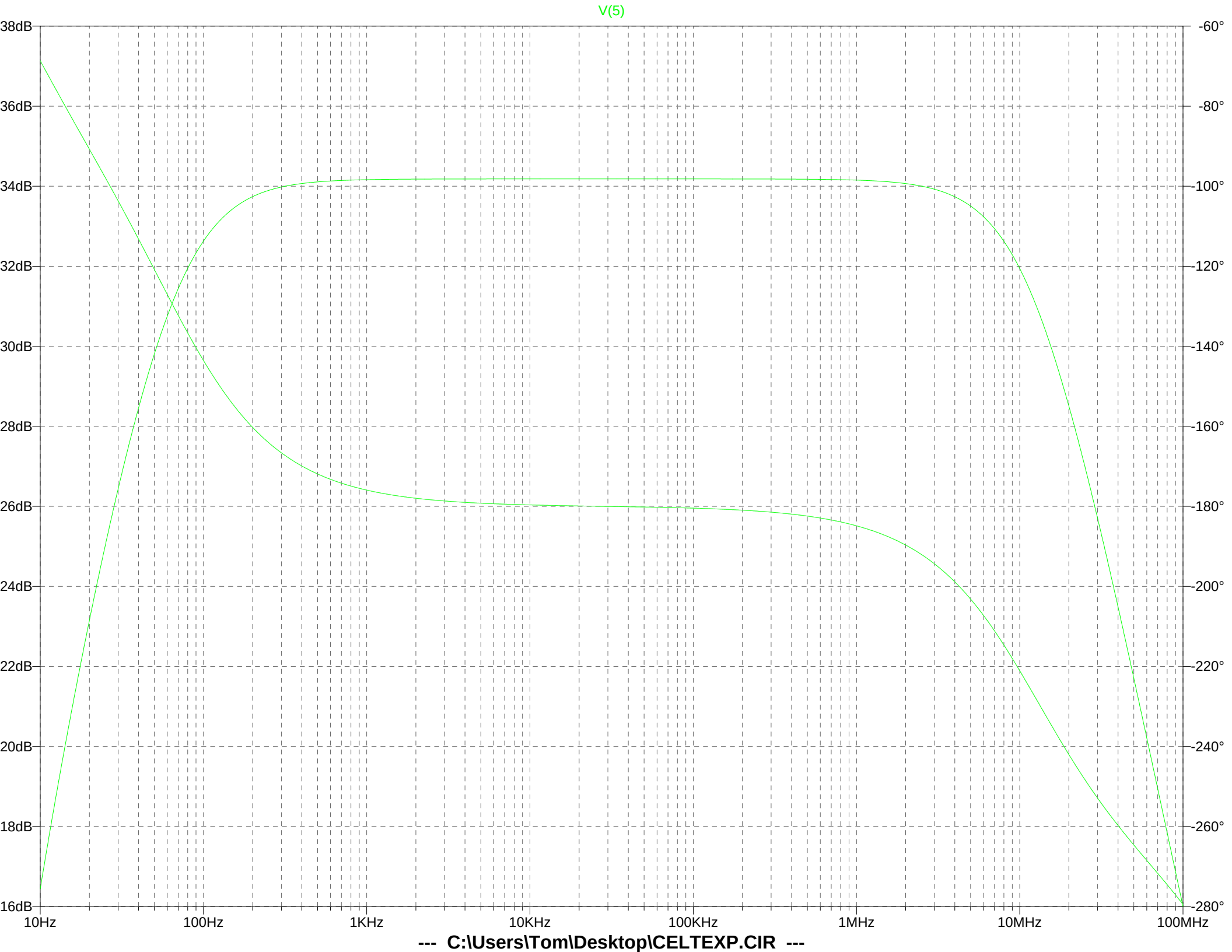
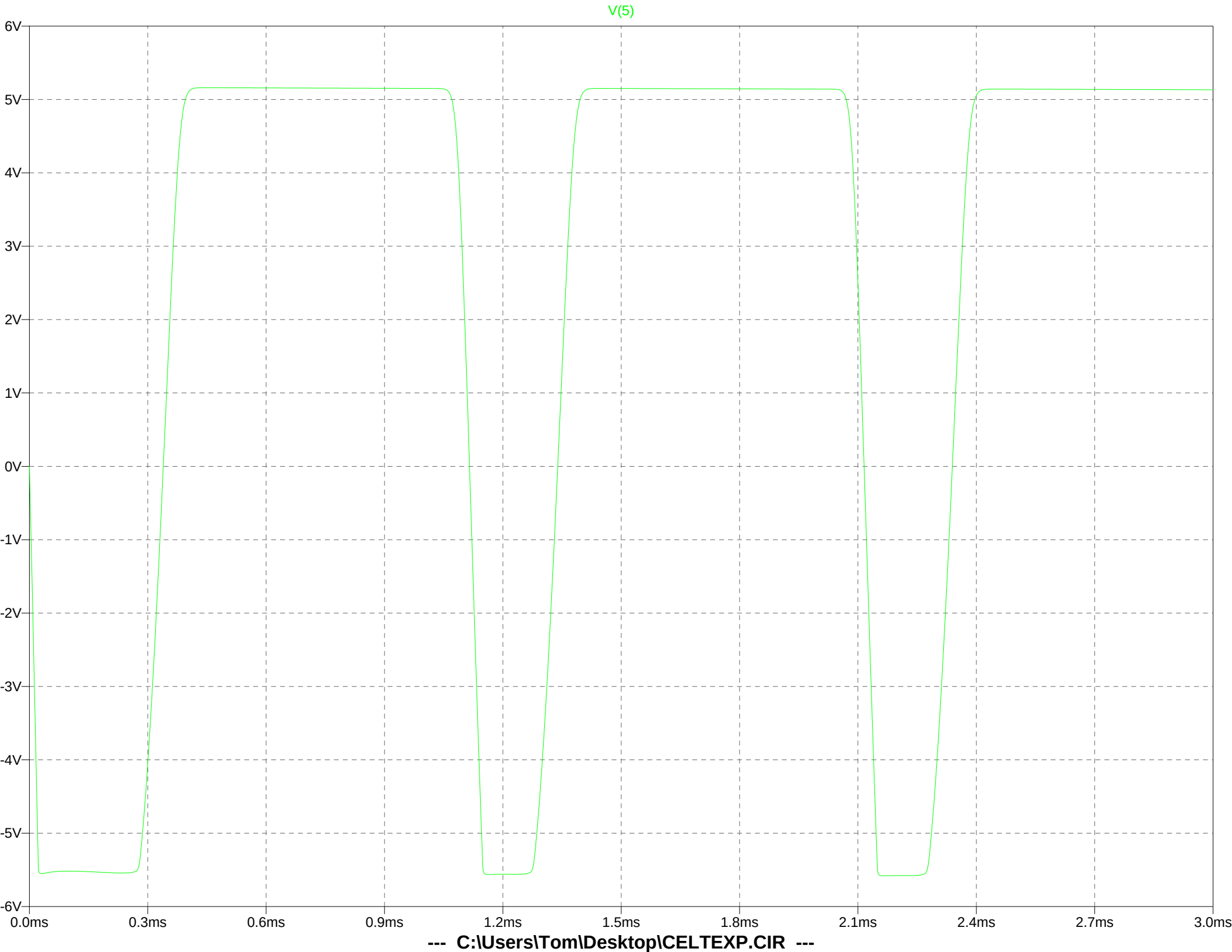
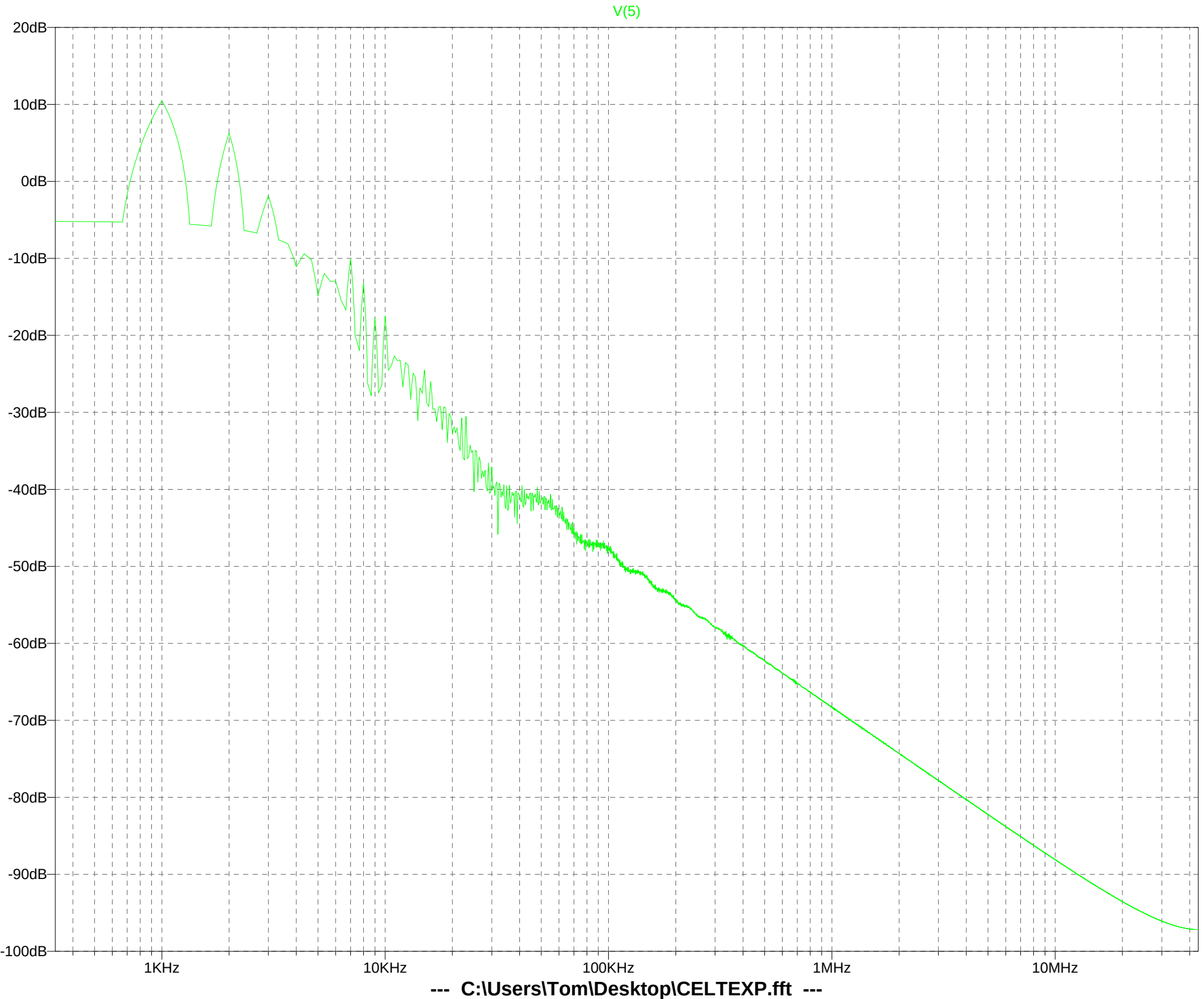

V(5)
38dB
36dB
34dB
32dB
30dB
28dB
26dB
24dB
22dB
20dB
18dB
16dB
-60°
-80°
-100°
-120°
-140°
-160°
-180°
-200°
-220°
-240°
-260°
-280°
10Hz
100Hz
1KHz
10KHz
100KHz
1MHz
10MHz
100MHz
--- C:\Users\Tom\Desktop\CELTEXP.CIR ---


V(5)
6V
5V
4V
3V
2V
1V
0V
-1V
-2V
-3V
-4V
-5V
-6V
0.0ms
0.3ms
0.6ms
0.9ms
1.2ms
1.5ms
1.8ms
2.1ms
2.4ms
2.7ms
3.0ms
--- C:\Users\Tom\Desktop\CELTEXP.CIR ---


V(5)
20dB
10dB
0dB
-10dB
-20dB
-30dB
-40dB
-50dB
-60dB
-70dB
-80dB
-90dB
-100dB
1KHz
10KHz
100KHz
1MHz
10MHz
--- C:\Users\Tom\Desktop\CELTEXP.fft ---